IN THE SPECIFICATION

Please amend the paragraph beginning on page 3, line 9 as follows:

The present application describes a 3D graphics accelerator which uses byte-tiled memory, and a high-speed image download path which provides higher bandwidth than the message-passing pipeline.

Please amend the paragraph beginning on page 5, line 5 as follows:

The present application describes a new graphics accelerator architecture (referred to herein as the [["P10:)]] "P10") which is different from conventional 3-D computer graphics architectures in several ways.

Please amend the paragraph beginning on page 34, line 24 as follows:

The primary cache is divided into two banks and each bank has 16 cache lines, each holding 16 texels in a 4x4 patch. The search is fully associative and 8 queries per cycle (4 in each bank) can be made. The replacement policy is LRU, but only on the set of cache lines not referenced by the current fragment or fragments in the latency FIFO. The banks are assigned so even mip map levels or 3D slices are in one bank while odd ones are in the other. The search key is based on the texel's index and texture ID not address in memory (saves having to compute 8 addresses). The cache coherency is only intended to work within a sub tile or maybe a tile and never between tiles.[[2]]

Please amend the paragraph beginning on page 44, line 21 as follows:

Additional disclosure is found in nonprovisional applications 10/071,895 filed Feb. 8, 2002 (TD-164), 10/071,896 filed Feb. 8, 2002 (TD-165), and 10/080,284 filed Feb. 20, 2002 (TD-169), all commonly owned, copending with the present application, and hereby incorporated by reference, and in provisional application Nos. 60/267,265, 60/267,266, 60/269,462, 60/269,463, 60/269,428, 60/269,802, 60/269,935, 60/271,851, 60/271,795, 60/271,796, 60/272,125, and 60/272,516, various of which are referenced in the nonprovisional filings cited above, and all of which are hereby incorporated by reference.